What is claimed is:

[Claim 1] A method of designing a programmable logic integrated circuit comprising:

taking a first layout of a programmable logic integrated circuit;
stretching the first layout using an edge of the first layout so the first layout has a stretched section;
taking a second layout of an embedded processor stripe for a programmable logic integrated circuit, wherein the embedded processor stripe comprises a watchdog timer circuit;
incorporating the second layout into stretched section of the first layout; and
coupling signal lines of the first layout to signal lines of the second layout.

[Claim 2] The method of claim 1 further comprising:

fabricating the programmable logic integrated circuit using a combination of the first and second layouts.

[Claim 3] A programmable logic integrated circuit designed according to the method recited in claim 1.

[Claim 4] A method comprising:

designing a layout of an embedded processor stripe to be incorporated into a programmable logic integrated circuit; and
including in the layout a watchdog timer circuit.

[Claim 5] The method of claim 4 further comprising:

including signal lines in the layout of the embedded processor stripe to be coupled to signal lines of a programmable logic portion of the programmable logic integrated circuit.

[Claim 6] The method of claim 4 wherein the layout is designed to be positioned at an edge of the programmable logic integrated circuit.

[Claim 7] A circuit comprising:

a programmable logic integrated circuit comprising an embedded processor portion and a programmable logic portion, wherein the embedded processor portion includes a watchdog timer circuit; and
an external configuration source integrated circuit, coupled to the programmable logic integrated circuit, storing configuration information for the programmable logic integrated circuit, wherein when the watchdog timer circuit asserts a triggered signal output due to not reloading the watchdog timer circuit within a timeout period, configuration data is loaded from the external configuration source into the programmable logic integrated circuit.

[Claim 8] The circuit of claim 7 wherein the external configuration source is a nonvolatile memory.

[Claim 9] The circuit of claim 7 wherein the watchdog timer circuit is reloaded by periodically loading a reload register of the watchdog timer with one or more magic values.

[Claim 10] The circuit of claim 7 wherein a configuration of the programmable logic portion of the programmable logic integrated circuit is held using volatile memory cells.

[Claim 11] The circuit of claim 10 wherein the volatile memory cells are SRAM cells.

[Claim 12] The circuit of claim 10 wherein configuration data from the external configuration source is used to configure the embedded processor portion and programmable logic portion of the programmable logic integrated circuit.

[Claim 13] The circuit of claim 7 wherein the configuration is transferred serially from the external configuration source to the programmable logic integrated circuit.

[Claim 14] The circuit of claim 7 wherein the watchdog timer circuit is not reloaded due to a software failure occurring within the embedded processor portion of the programmable logic integrated circuit.

[Claim 15] The circuit of claim 7 wherein the watchdog circuit is not reloaded due to a power supply problem.

[Claim 16] A programmable logic integrated circuit comprising:

a programmable logic portion of the integrated circuit comprising a plurality of logic array blocks, configurable to perform user logic, wherein the logic array blocks are arranged in rows and columns; and
an embedded processor portion of the integrated circuit, coupled to the programmable logic portion, comprising a watchdog timer circuit which is triggered if a count register of the watchdog timer circuit is permitted to count to a final value before the count register is reloaded.

[Claim 17] The programmable logic integrated circuit of claim 16 wherein triggering of the watchdog timer circuit is avoided when the watchdog timer circuit is periodically reloaded, before a timeout period, by writing a magic value to a reload register.

[Claim 18] The programmable logic integrated circuit of claim 17 wherein the timeout period is a time it takes for the watchdog timer circuit to count from an initial value to the final value.

[Claim 19] The programmable logic integrated circuit of claim 16 wherein the plurality of logic array blocks are configured by programming SRAM memory cells.

[Claim 20] The programmable logic integrated circuit of claim 16 wherein the plurality of logic array blocks are configured by programming volatile memory cells.

[Claim 21] The programmable logic integrated circuit of claim 16 wherein the watchdog timer circuit comprises a reload register and a control register.

[Claim 22] The programmable logic integrated circuit of claim 16 wherein each logic array block comprises a look-up table circuit.

[Claim 23] The programmable logic integrated circuit of claim 16 wherein after the watchdog timer circuit is triggered, a reset circuit of the programmable logic integrated circuit effects loading of configuration data from an external source to reconfigure the programmable logic and embedded processor position of integrated circuit.

[Claim 24] The programmable logic integrated circuit of claim 16 wherein the embedded processor portion further comprises a central processing unit and an embedded processor memory block, coupled together using a first bus.

[Claim 25] The programmable logic integrated circuit of claim 24 wherein the watchdog timer circuit is also coupled to the first bus.

[Claim 26] The programmable logic integrated circuit of claim 24 wherein the embedded processor further comprises a second bus, through which the memory block is coupled to the programmable logic portion of the integrated circuit.

[Claim 27] The programmable logic integrated circuit of claim 24 wherein the external source is a Flash memory, EPROM memory, nonvolatile memory, or serial memory.

[Claim 28] The programmable logic integrated circuit of claim 23 wherein the configuration data is transferred to the programmable logic integrated circuit by using a serial stream of bits.